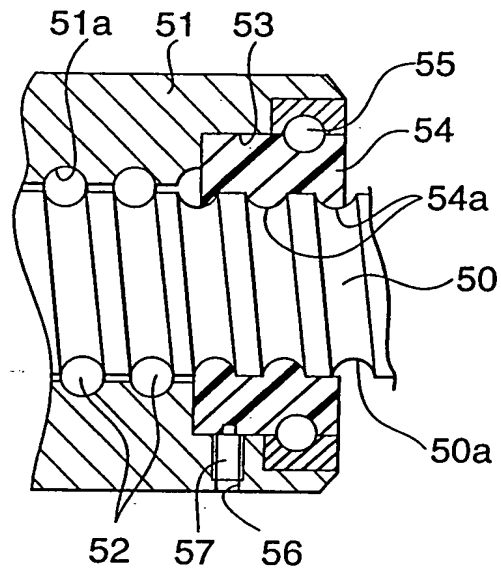
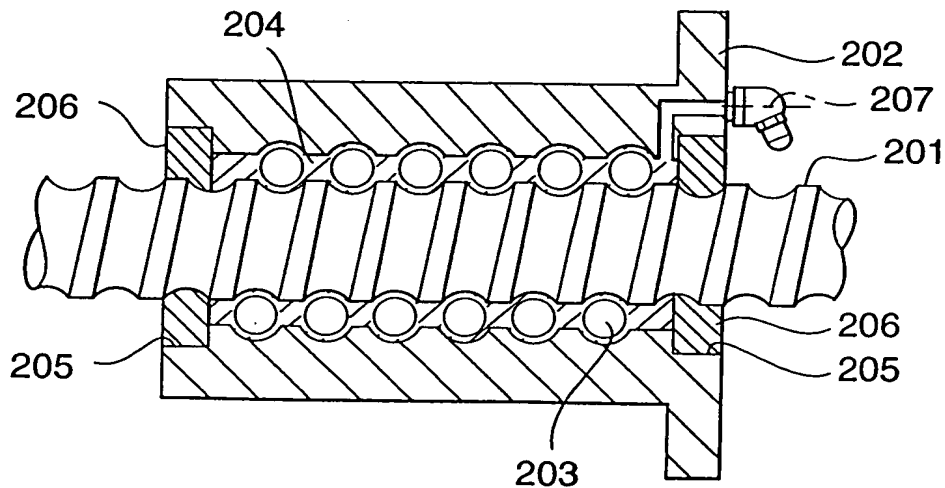
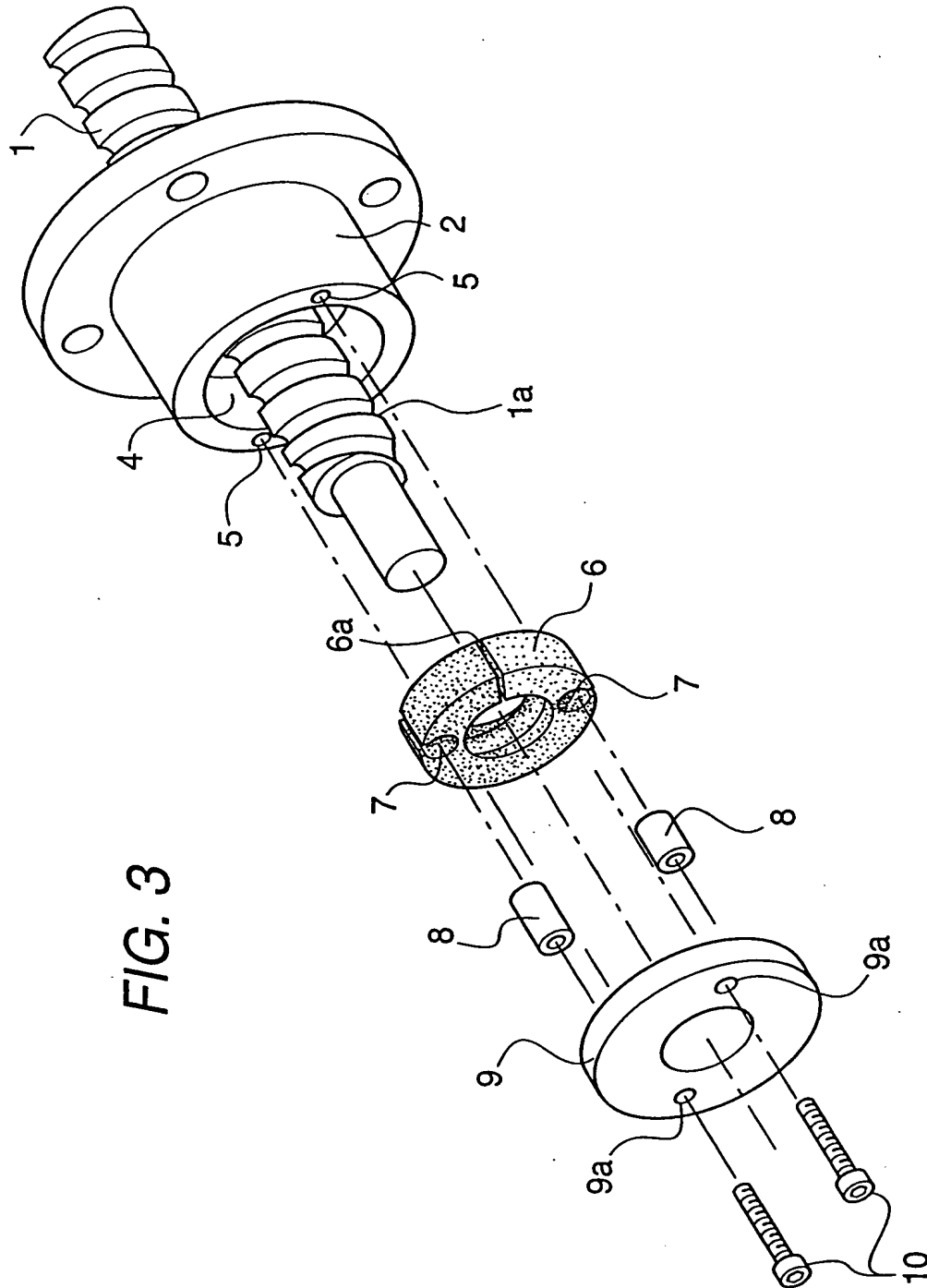


**FIG. 1**  
**PRIOR ART**

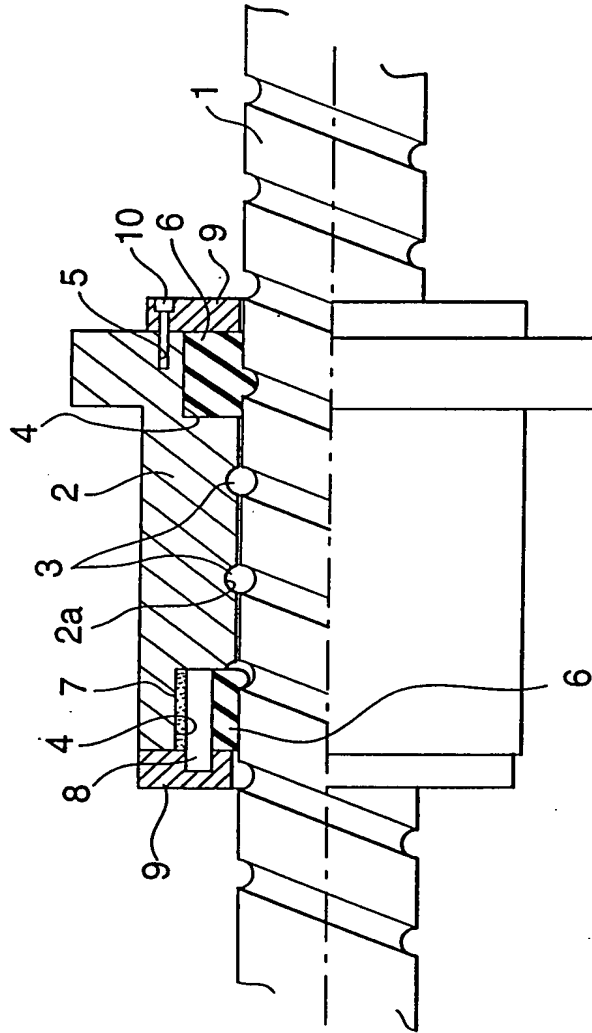


**FIG. 2**  
**PRIOR ART**

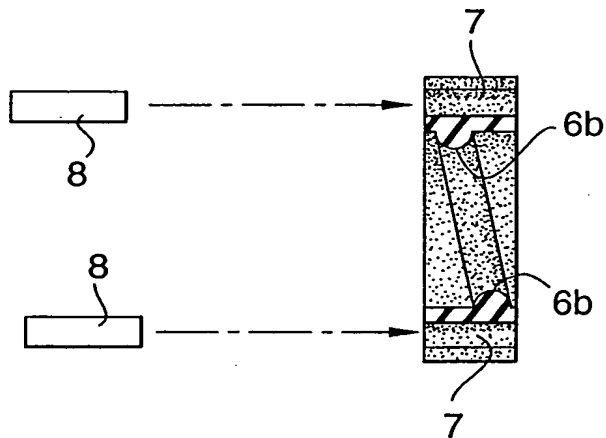




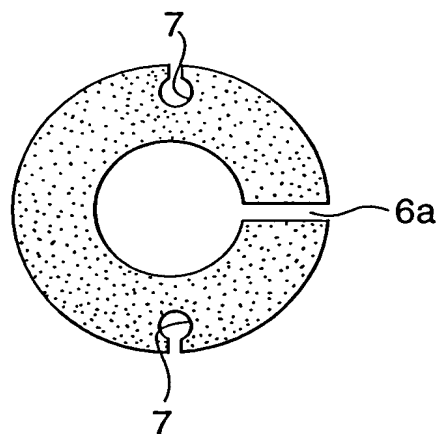
**FIG. 4**



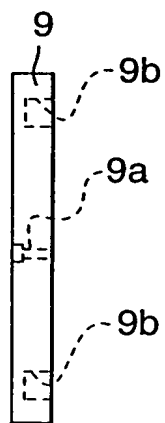
*FIG. 5 (a)*



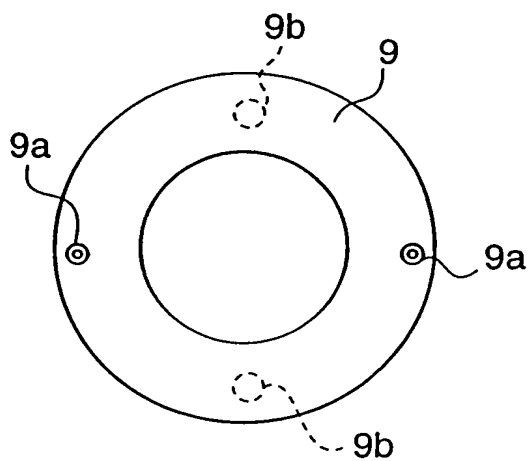
*FIG. 5 (b)*



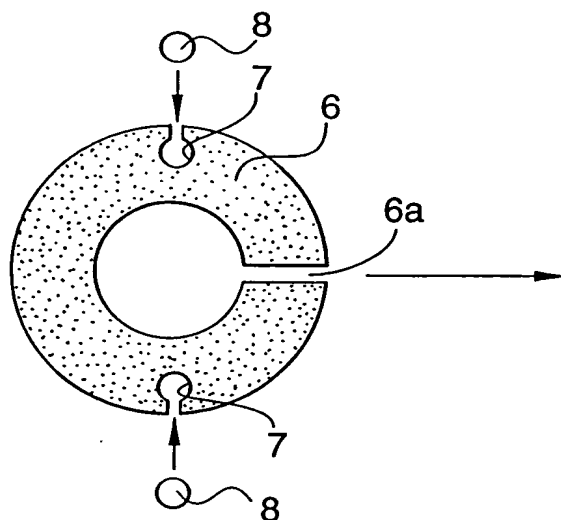
*FIG. 6 (a)*



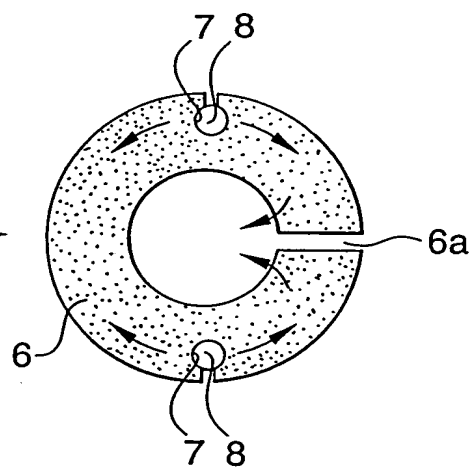
*FIG. 6 (b)*



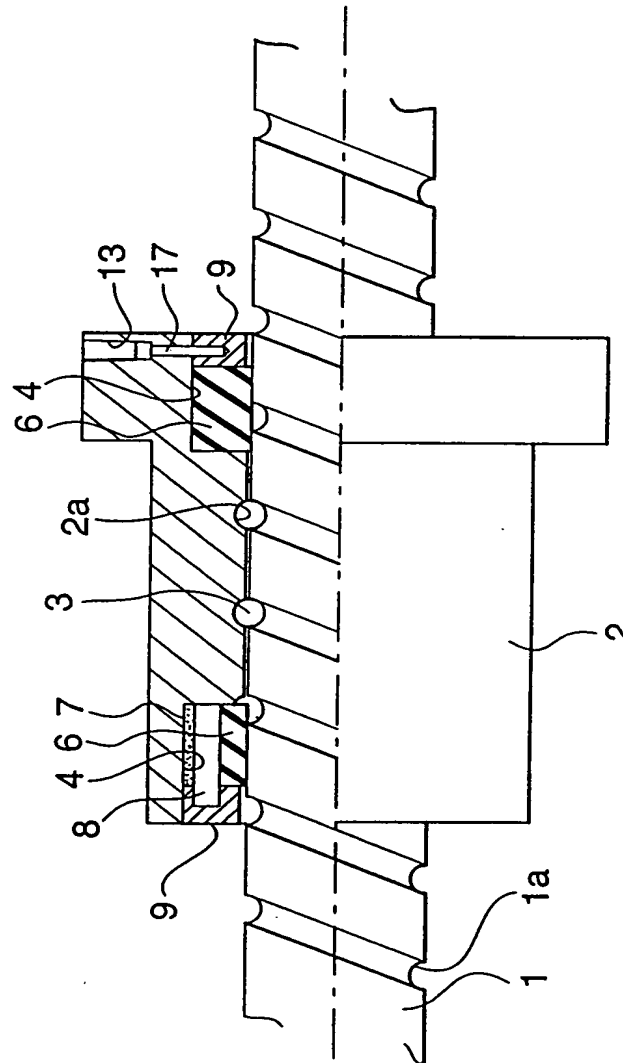
*FIG. 7 (a)*



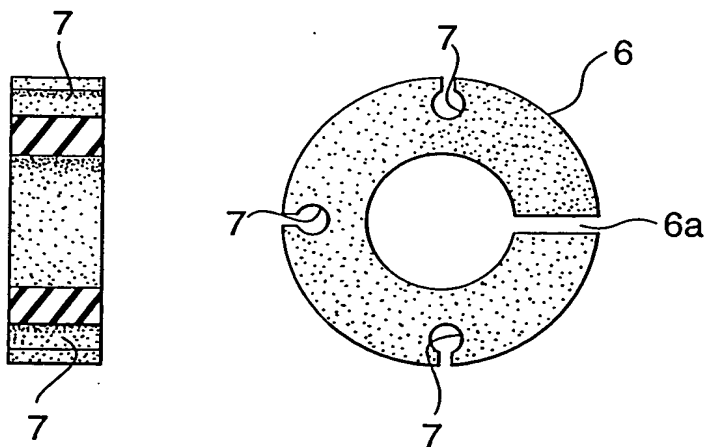
*FIG. 7 (b)*



**FIG. 8**



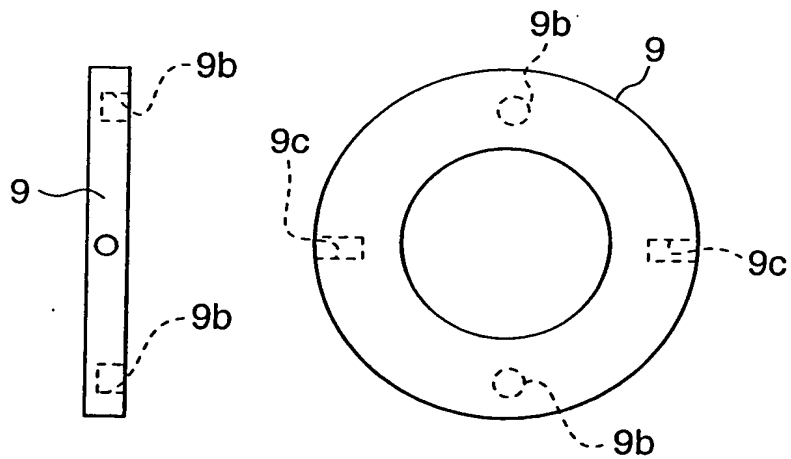
*FIG. 9 (a)*      *FIG. 9 (b)*

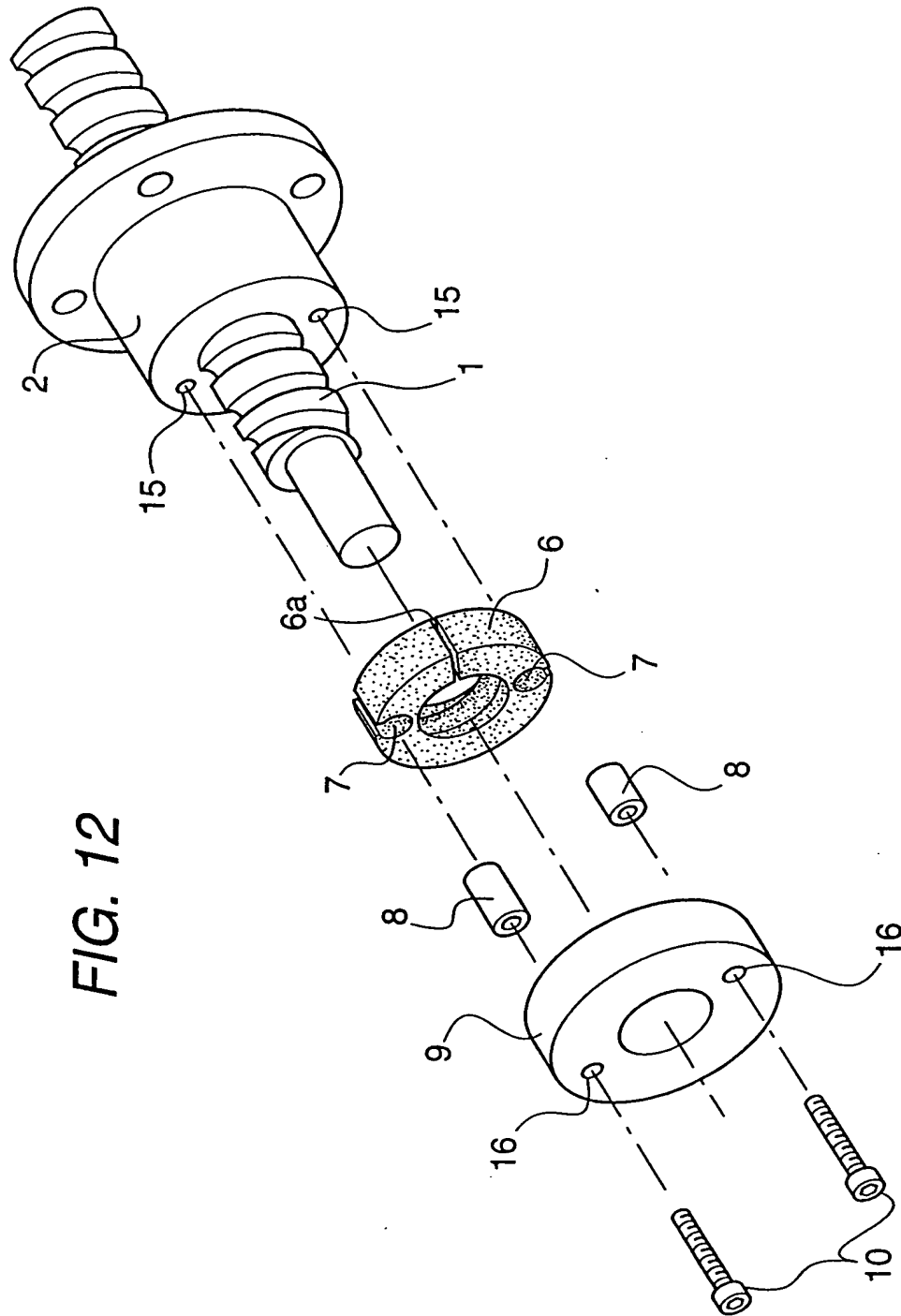


*FIG. 10 (a)*      *FIG. 10 (b)*



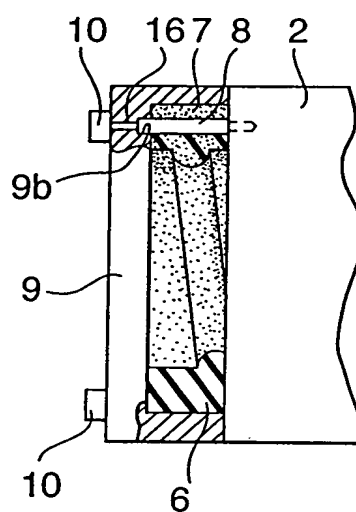
*FIG. 11 (a)*      *FIG. 11 (b)*







**FIG. 13**



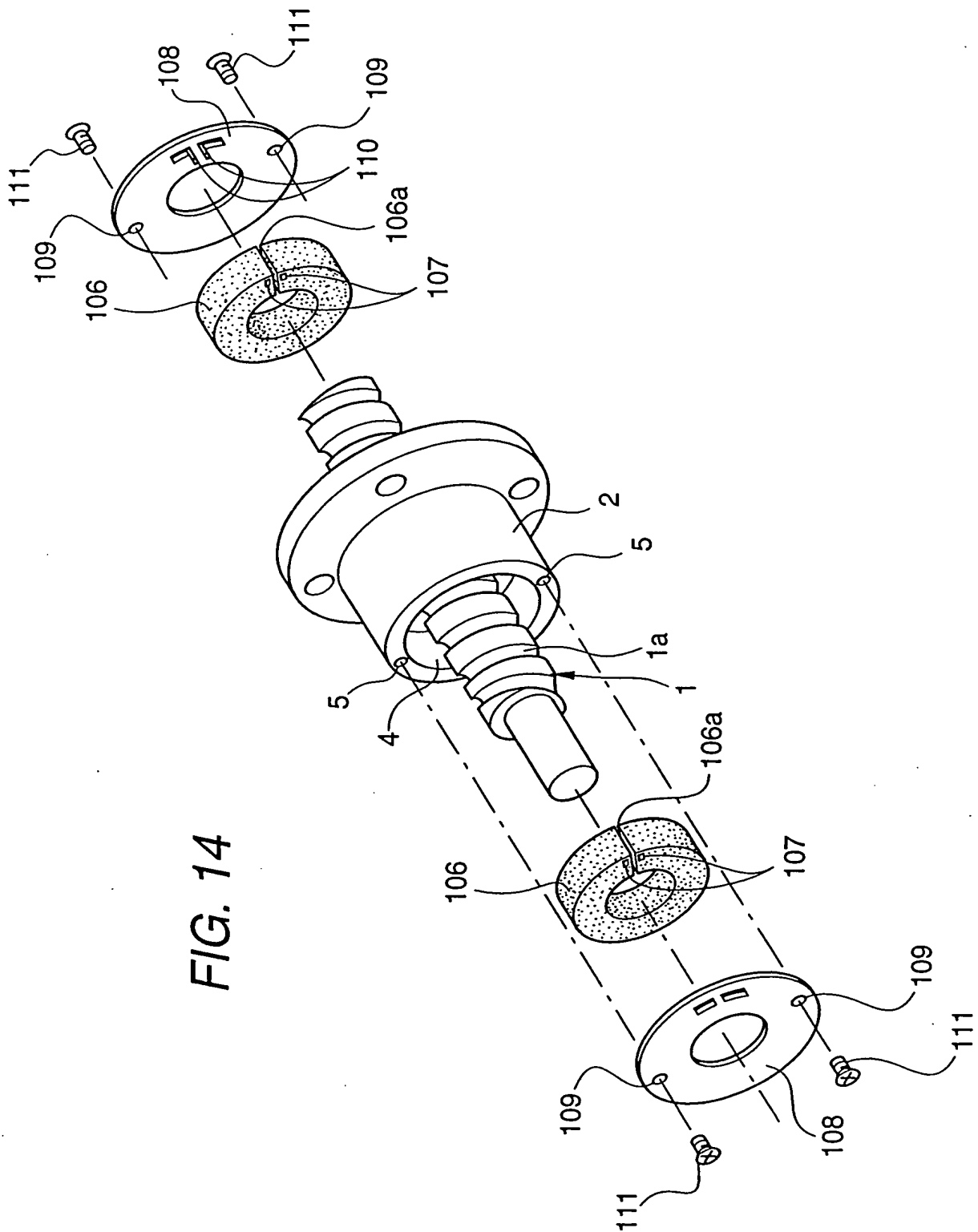
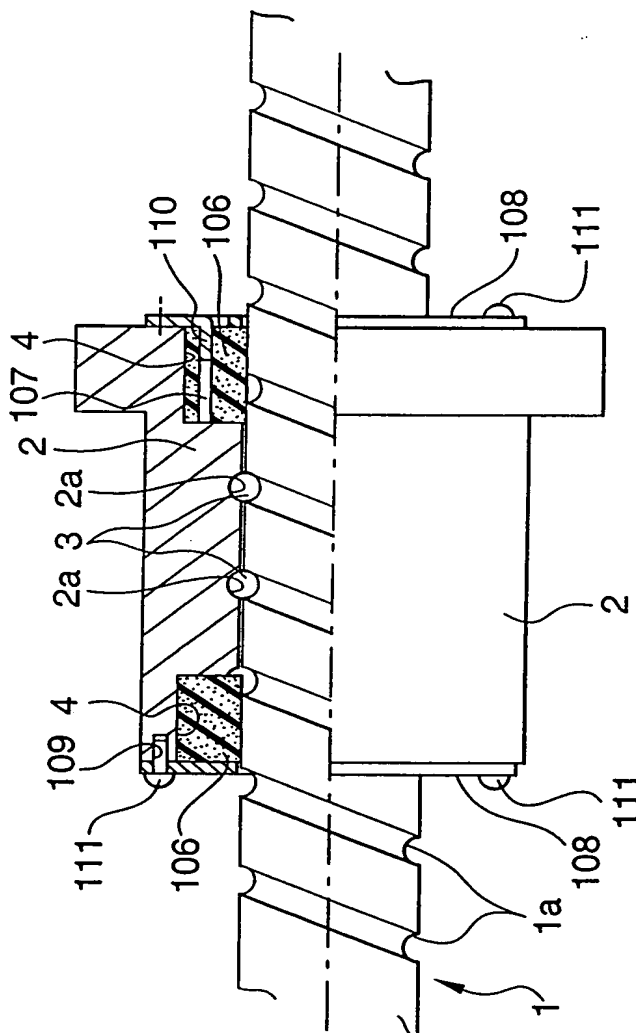
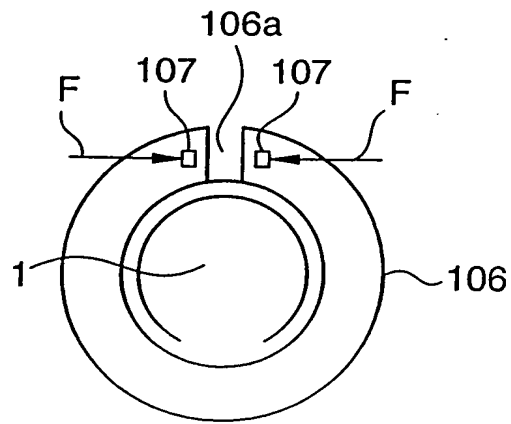


FIG. 15



**FIG. 16**



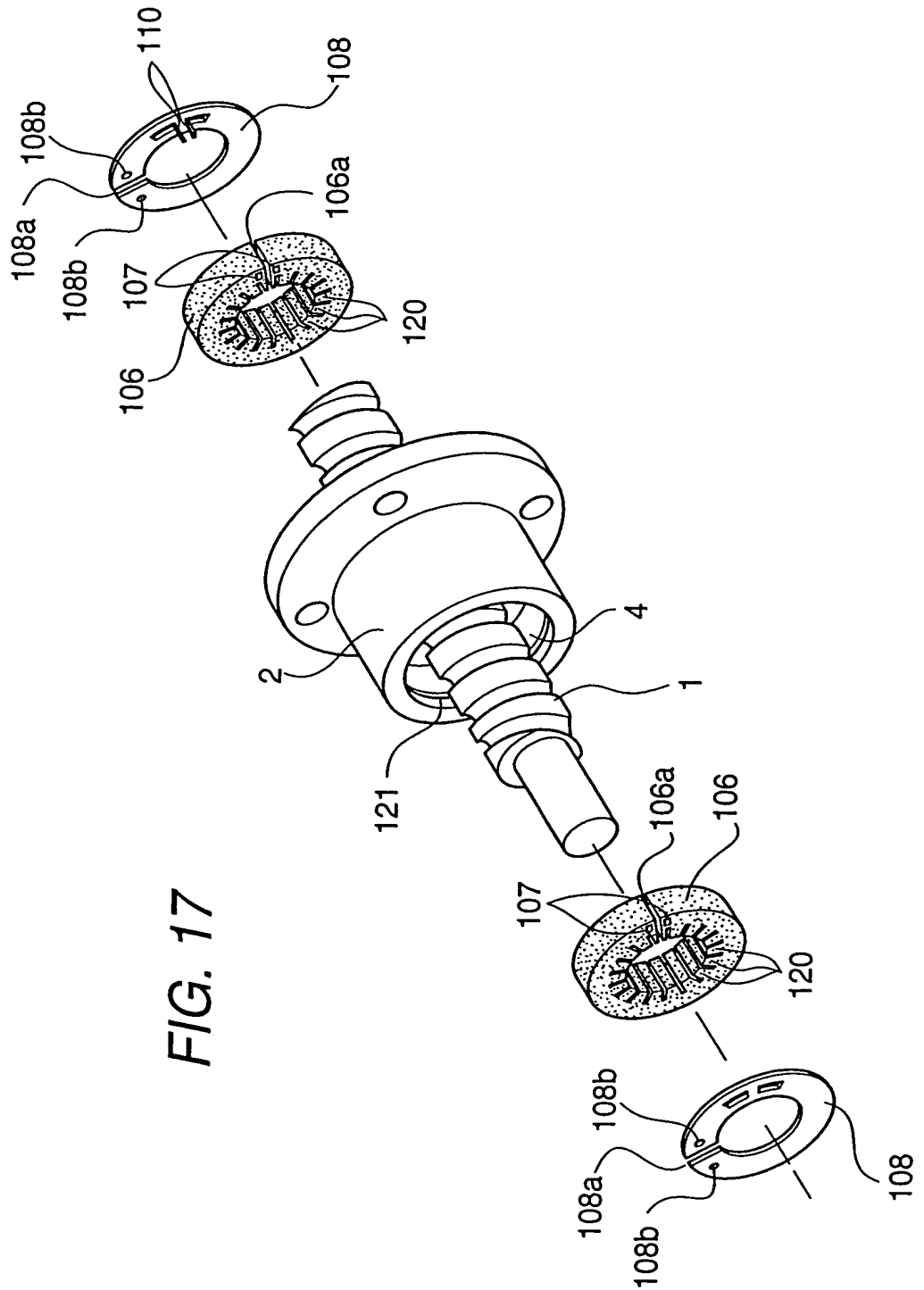
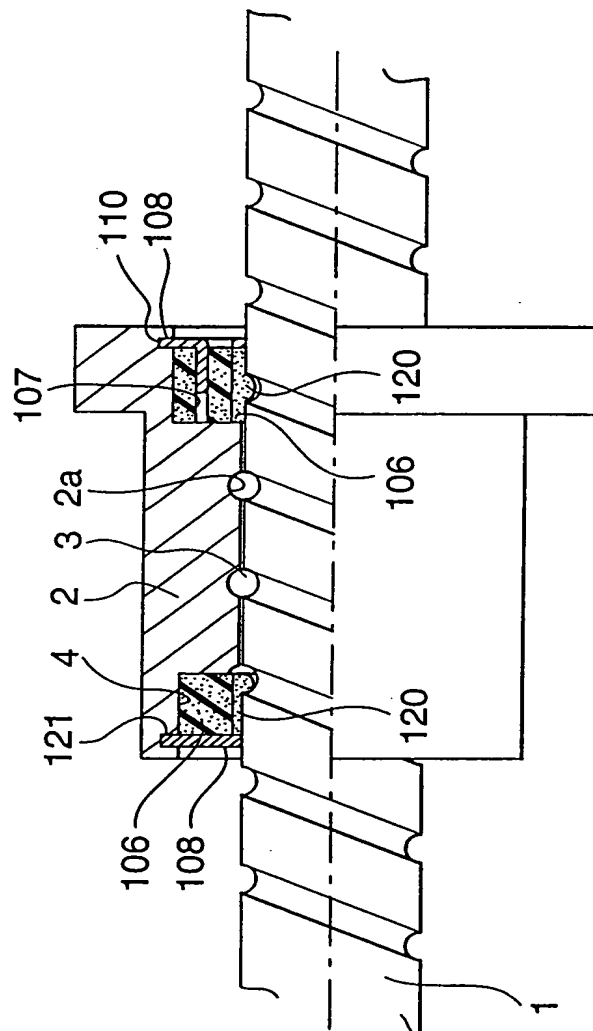
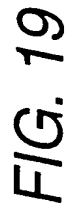
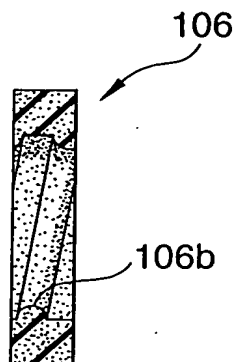


FIG. 18

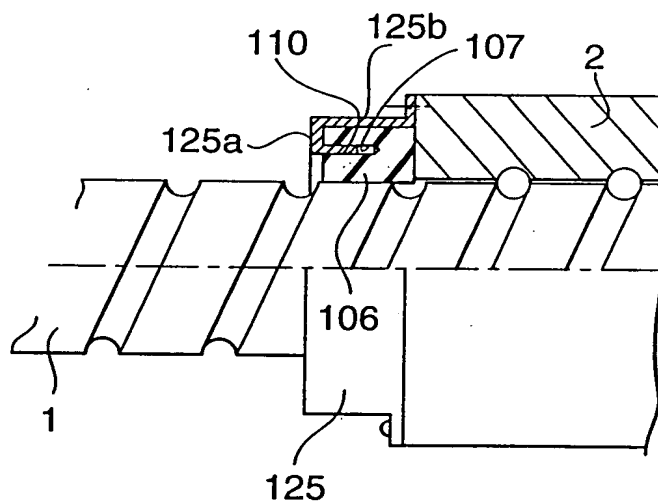




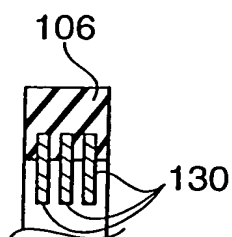
**FIG. 20**



**FIG. 21**

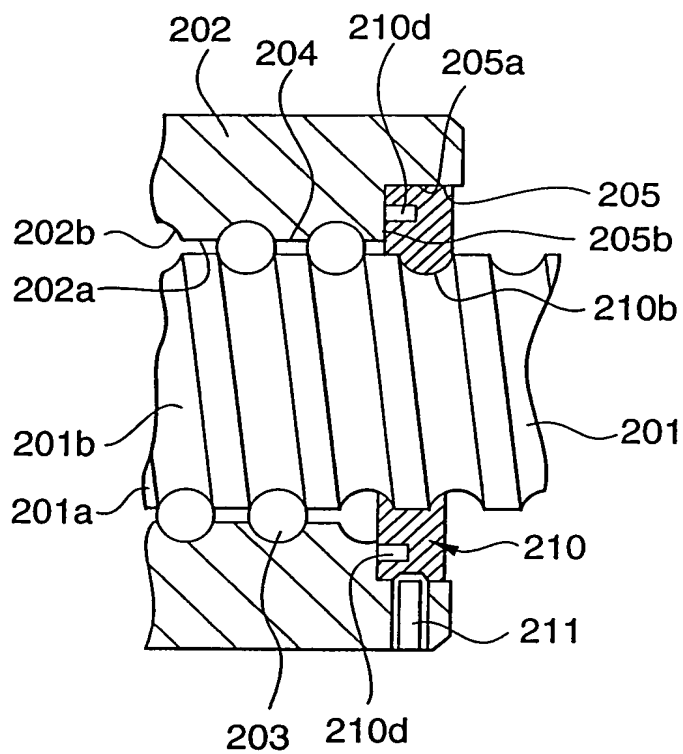


**FIG. 22**

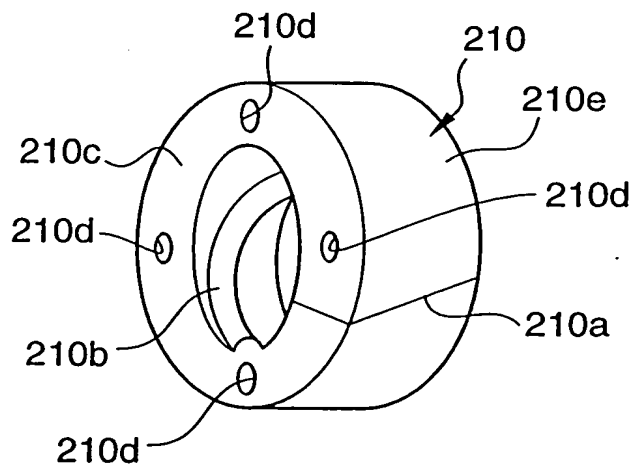




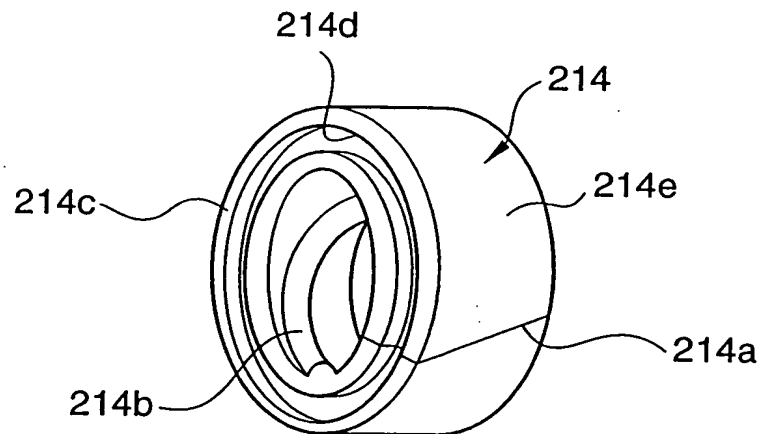
**FIG. 23**



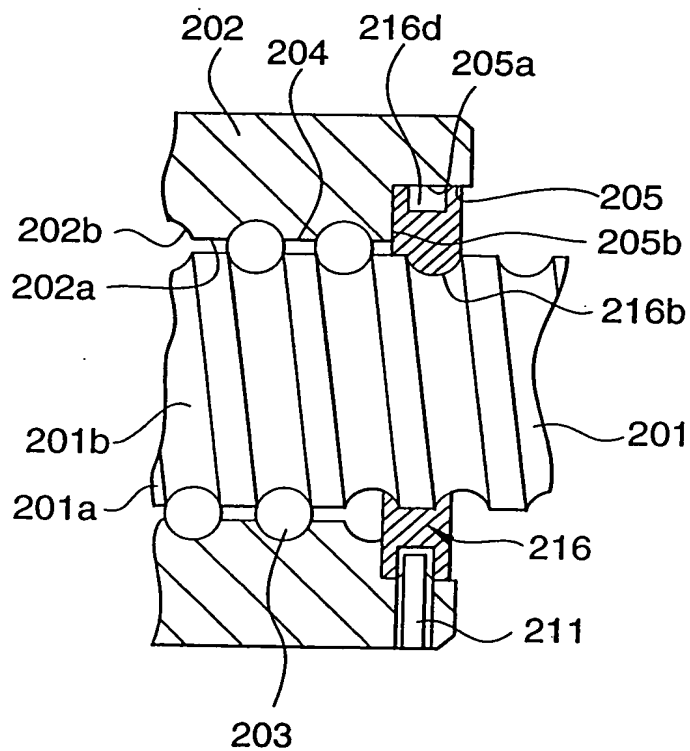
**FIG. 24**



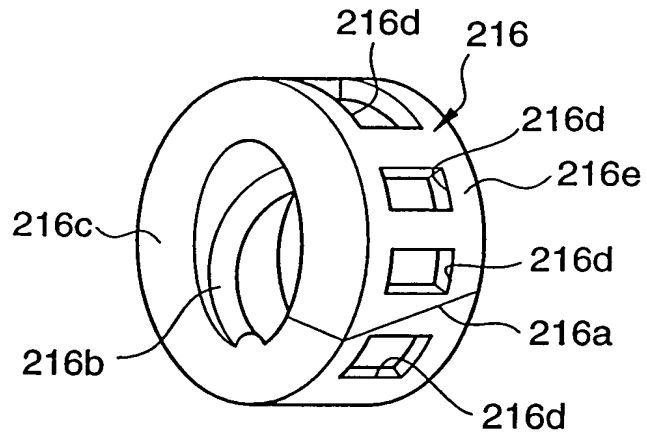
**FIG. 25**



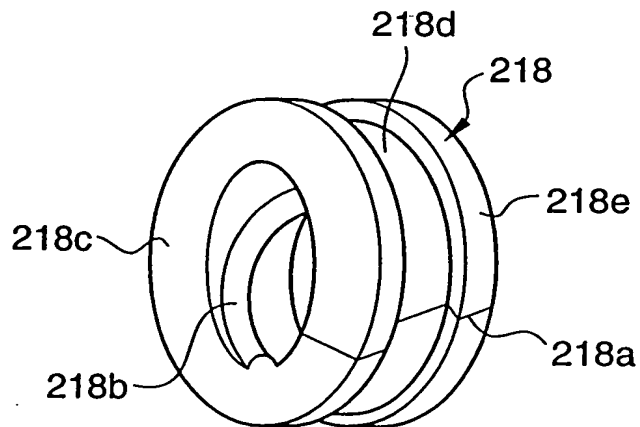
**FIG. 26**



**FIG. 27**

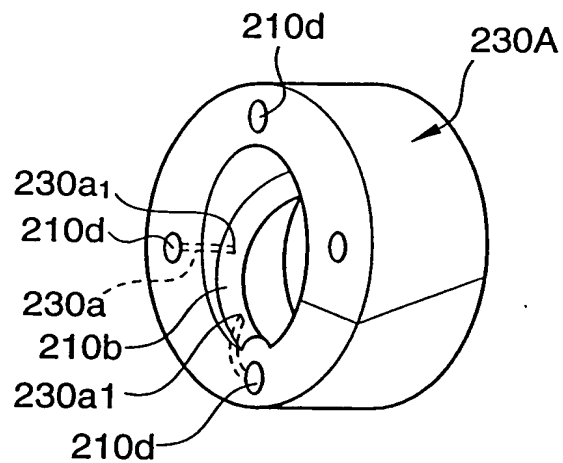


**FIG. 28**

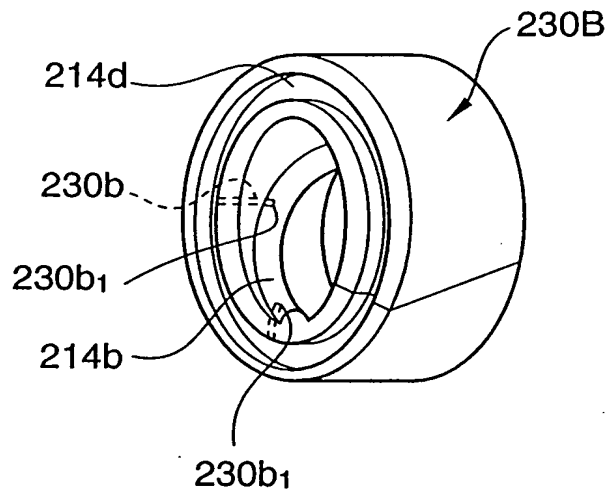


This cross-sectional diagram illustrates a semiconductor device with several distinct layers and components. At the top, a layer labeled 205b is shown above a layer 205. Below these are layers 222c and 222. A central region contains vertical structures 201a and 201b, which are separated by circular features 202a and 202b. These vertical structures are supported by a base layer 203. To the right, there are additional layers 224 and 220d, with a dashed line indicating a boundary or interface. The bottom of the device shows a substrate 211 and a layer 220f. Various other labels like 202, 204, 205, 222a, 220b, and 224 point to specific regions and interfaces within the device.

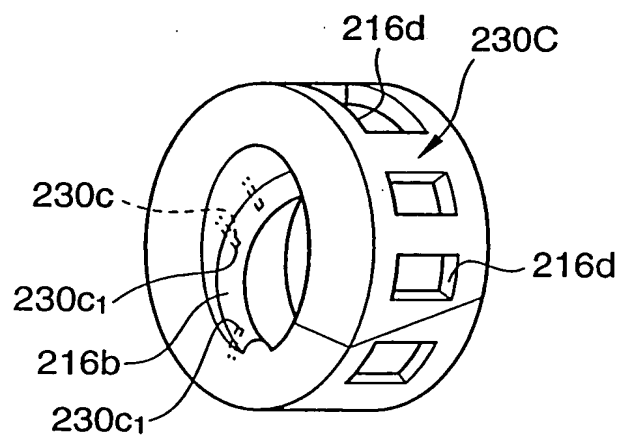
**FIG. 31**



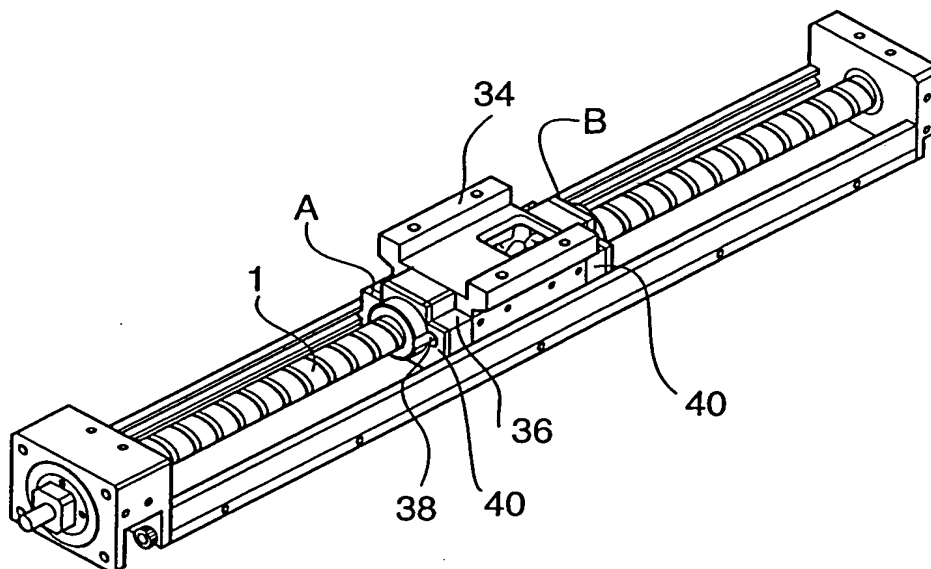
**FIG. 32**



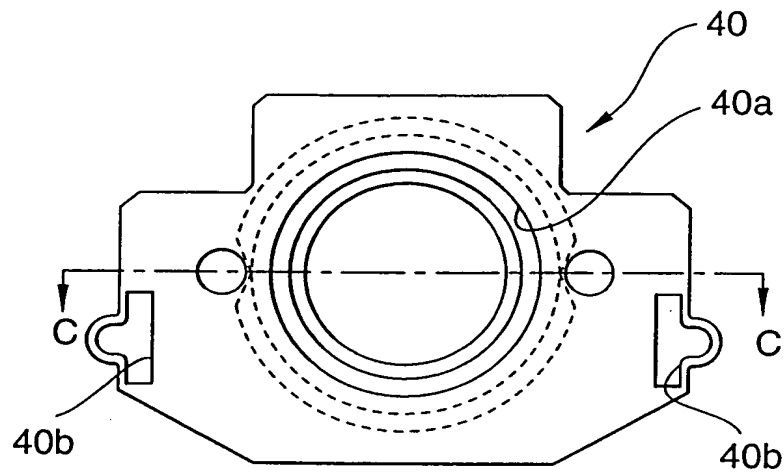
**FIG. 33**



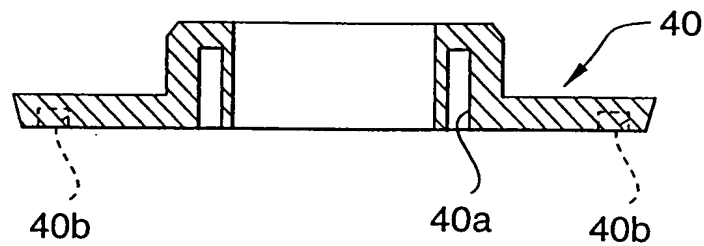
**FIG. 34**



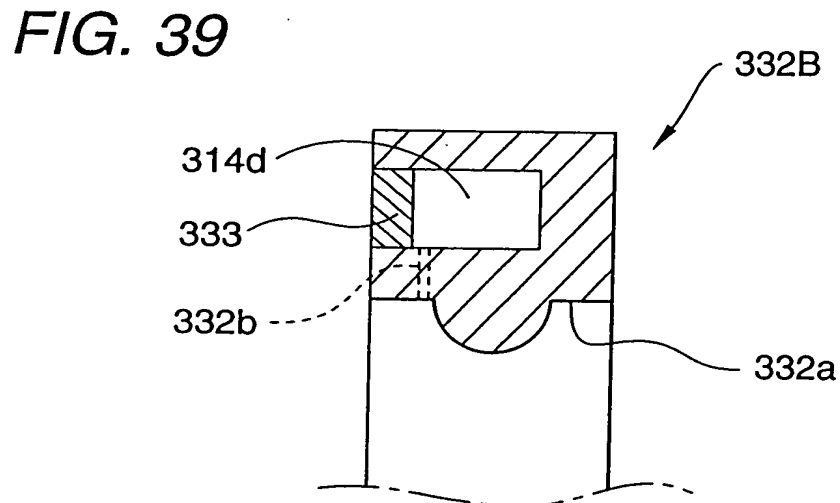
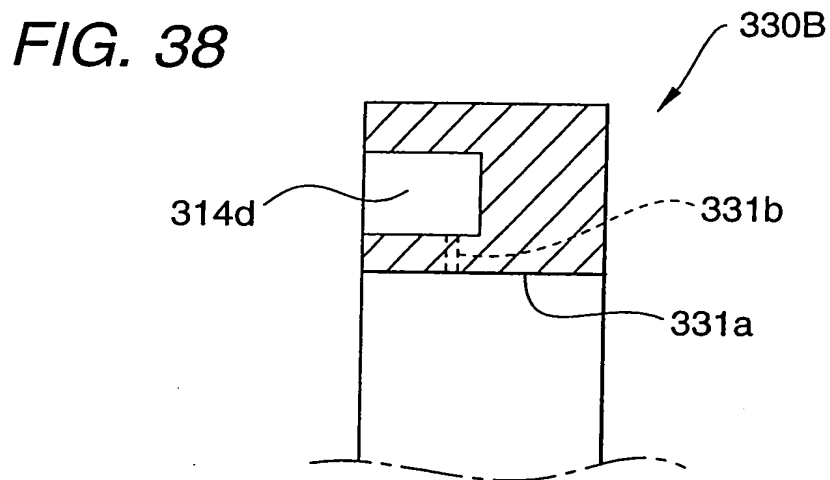
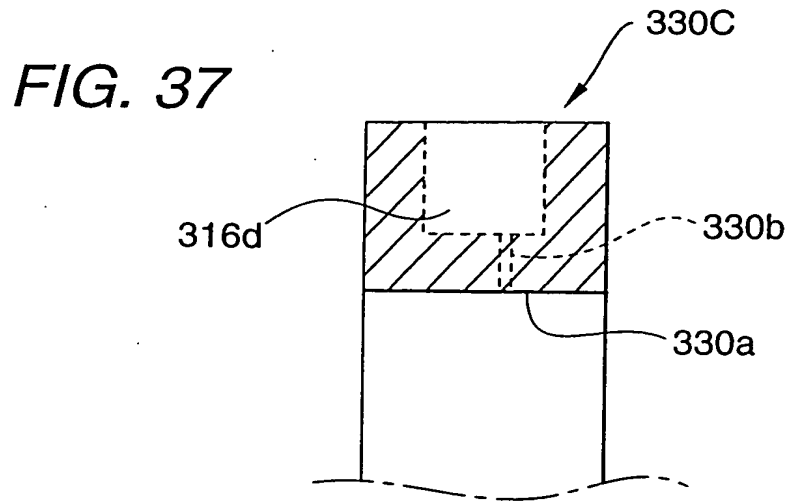
**FIG. 35**



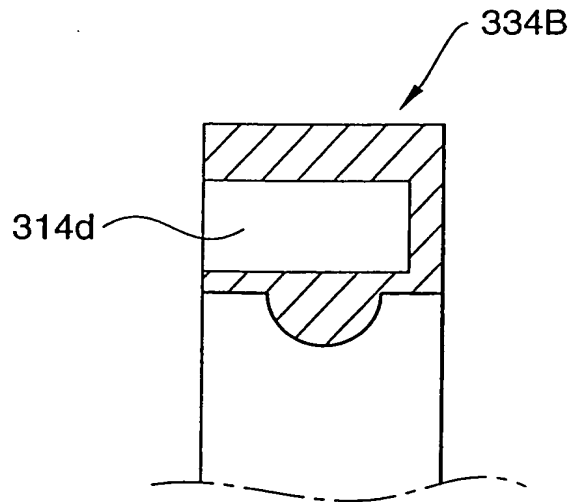
**FIG. 36**







**FIG. 40**



**FIG. 41**

